Remarks

Reconsideration of the above-identified application is requested in view of the remarks that follow. Since this response has been filed within two months after the September 9, 2005, mailing date of the Final Rejection in this application, a timely Advisory Action is requested.

The Examiner has repeated his rejection of claims 1-8, as amended, under 35 U.S.C. 103(a) as being unpatentable over the Choi et al. reference in view of the Ichikawa reference. In so doing, the Examiner states that it would be obvious to a person skilled in the art to modify the Choi et al. MOSFET transistor structure to provide Applicant's claimed invention. The Examiner has made this rejection "final."

Applicant has again amended independent MOSFET transistor structure claim 1 and independent method claim 7 to more clearly define the invention. Language has been added to both independent claim 1 and independent claim 7 to reflect the structure shown in Fig. 3A of the application and a method of making the Fig. 3A structure. Specifically, claims 1 and 7 have been amended to recite not only that the active region formed in the substrate of the semiconductor material is substantially rectangular, thereby defining a substantially rectangular interface between the active region and the isolation dielectric material, but also that the conductive gate electrode includes two openings formed therethrough, one over the source region and one over the drain region. Both claim 1 and claim 7 further recite that the conductive gate is formed to include a first portion that extends over the substrate channel region of the MOSFET transistor and second portion that extends continuously over the entire substantially rectangular perimeter interface between the isolation dielectric material and the active region.

Upon close review of the Choi et al. reference and the Ichikawa reference, Applicant submits that neither reference, whether considered individually or in combination, either teaches or suggests the formation of a MOSFET transistor conductive gate electrode as shown in Applicant's Fig 3A, i.e., a rectangular gate electrode that extends continuously over the entire substantially rectangular interface between isolation dielectric material and a substantially rectangular active device region for the MOSFET transistor and is open over the source and drain regions of the MOSFET transistor. The "gate electrode" referenced by the Examiner as taught by the Choi et al. publication is actually the word line of a non-volatile memory cell array

structure and has no structural similarities to the gate electrode recited in Applicant's claims 1 and 7. Likewise, the gate electrode structure cited by the Examiner with respect to the Ichikawa reference has very little structural similarity to the conductive gate electrode recited in Applicant's claims 1 and 7, lacking the rectangular features as well as the source-drain openings, among others. While Applicant disputes that there is motivation in either reference for combining a non-volatile memory word line structure and a MOS transistor structure to somehow arrive at Applicant's claimed invention, any resulting combination would still be lacking in features set forth in Applicant's claims 1 and 7.

Applicant notes that the claim 1 structure and the claim 7 method are also applicable to the CMOS transistor structure shown in Applicant's Fig. 4A.

In view of the above, Applicant submits that all claims now present in this application patentably distinguish over the prior art. Therefore, it is requested that this application be pass to allowance.

Respectfully submitted,

STALLMAN & POLLOCK LLP

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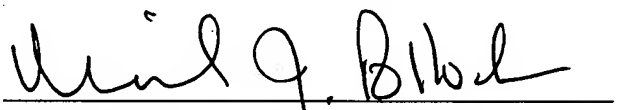
By: 

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